WHAT IS CLAIMED IS:

1. A method for recovering at least one of a correct phase and frequency clock for an analog video signal that is converted for display on a digital display object having pixels arranged in lines and columns, the analog video signal including an analog video data signal with pixel components being generated at a pixel component frequency, the analog video data signal being generated to produce frames of analog video data, each frame being made up of a plurality of lines of pixel components, with each line having a central active video region made up of activated pixel components, the central active video region having edges surrounded by inactive blanked regions made up of inactive pixel components, the method comprising the steps of:

generating a pixel clock waveform having a series of pixel clock pulses, the pixel clock pulses having portions operable to sample values of the analog video signal;

sampling values of the analog video signal pixel components with the pixel clock pulses;

selecting a ~~selected~~ pixel component adjacent the edge of the central active video region that is horizontally stationary from frame to frame of analog video data; and

automatically iteratively adjusting a phase of the pixel clock pulses until a pixel clock pulse is centrally registered with the selected pixel component.

2. A method for recovering a correct phase clock for an analog video signal that is converted for display on a digital display object having pixels arranged in lines and columns, the analog video signal including an analog video data signal with pixel components being generated at a pixel component frequency, the analog video data signal being generated to produce frames of analog video data, each frame being made up of a plurality of lines of pixel components, with each line having a central active video region made up of activated pixel components and inactive blanked regions made up of inactive pixel components on either side of the central active region, the method comprising the steps of:

generating a pixel clock waveform having a series of pixel clock pulses, the pixel clock pulses having a clock frequency that is equal to the pixel component frequency of the analog video signal;

sampling values of the analog video signal with the pixel clock pulses;

designating the pixel clock pulses that sample each line of analog video data with consecutive numbers;

identifying a selected number of the consecutive numbers that is associated with a pixel clock pulse that samples a selected pixel component in the frames of analog video data, wherein the selected pixel component is horizontally stationary from frame to frame of analog video data;

iteratively adjusting a pixel clock pulse phase for each of a series of frames until the selected number associated with the selected pixel component shifts by one integer to a shifted number, and further until the shifted number associated with the selected pixel component shifts back to the selected number;

identifying a subseries of frames within the series of frames, wherein each of the subseries of frames is associated with the shifted number;

identifying a corrected phase setting associated with a frame at the center of the subseries of frames associated with the shifted number; and

setting the pixel clock pulse phase component to the corrected phase setting.

3. The method of claim 2, wherein the selected pixel component is positioned in the active video region immediately adjacent one of the inactive blanked regions.

4. The method of claim 2, wherein the selected pixel component is a left-hand-most active pixel component.

5. The method of claim 2, wherein the shifted number is one integer different than the selected number.

6. The method of claim 2, wherein the selected pixel component is selected by the steps of:

selecting a threshold pixel value;

calculating values for the pixel components; and

comparing the values with the threshold pixel value.

7. The method of claim 6, wherein the selected pixel component has a value that is greater than the threshold pixel value.

8. The method of claim 6, wherein a first pixel component that is sampled in a frame of analog video data that has a calculated value greater than the threshold value is selected as the selected pixel component.

9. The method of claim 2, wherein the clock frequency is set equal to the pixel component frequency by the steps of:

estimating an expected width E, measured in number of pixel clock pulses, of an expected video image producible by the analog video signal;

calculating an actual width W, measured in number of pixel clock pulses, of an actual video image producible by the analog video signal;

comparing the actual width W with the expected width E; and

automatically adjusting the clock frequency whenever one of $W > E + 1$ and $W < E$.

10. The method of claim 9, wherein the clock frequency is decreased whenever $E < W - 1$.

11. The method of claim 9, wherein the clock frequency is increased whenever $E > W$.

12. The method of claim 8, wherein the clock frequency is adjustable by adjusting a number *n* of pixel clock pulses across each line in a frame of video data.

13. A system for recovering a correct phase clock for an analog video signal that is converted for display on a digital display object having pixels arranged in lines and columns, the analog video signal including an analog video data signal with pixel components being generated at a pixel component frequency, the analog video data signal being generated to produce frames of analog video data, each frame being made up of a plurality of lines of pixel components having a central active video region defined by edges that are surrounded by regions made up of inactive pixel components, the system comprising:

a pixel clock signal generator for generating pixel clock pulses, the pixel clock pulses having portions that sample values of the analog video signal pixel components;

a pixel component selection means for identifying a selected pixel component adjacent the edge of the central active video region that has a constant horizontal position from frame to frame;

a programmable delay device operable to automatically and iteratively adjust a phase of the pixel clock pulses until a pixel clock pulse portion is centrally registered with the selected pixel component.

14. A system for recovering a correct phase clock for an analog video signal that is converted for display on a digital display object having pixels arranged in lines and columns, the analog video signal including an analog video data signal with pixel components being generated at a pixel component frequency, the analog video data signal being generated to produce frames of analog video data, each frame being made up of a plurality of lines of pixel components, with each line having a central active video region made up of activated pixel components and inactive blanked regions made up of inactive pixel components on either side of the central active region, the system comprising:

a pixel clock signal generator for generating pixel clock pulses at a clock frequency that is equal to the pixel component frequency of the analog video signal, the pixel clock pulses sampling values of the analog video signal;

a counter operable to apply consecutive numbers to the pixel clock pulses that sample each line of pixel components;

a pixel component value comparator that identifies a selected pixel component based on a value of the selected pixel component, the selected pixel component having a constant horizontal position from frame to frame;

the counter operable to apply a selected number of the consecutive numbers to a pixel clock pulse that samples the selected pixel component;

a programmable delay device operable to iteratively adjust a phase of the pixel clock pulses for each of a series of frames until the selected number associated with the selected pixel component shifts by one integer to a shifted number, and further until the shifted number shifts back to the selected number;

a memory device operable to consecutively store the selected numbers and shifted numbers of the series of frames;

means for selecting a subseries of frames from the series of frames, the subseries of frames being associated with the shifted number, for selecting a corrected phase setting associated with a frame at the center of the subseries of frames, and for setting the pixel clock pulse phase component to the corrected phase setting.

15. The system of claim 14, wherein the selected pixel ~~clock~~ component is positioned in the active video region immediately adjacent one of the inactive blanked regions.

16. The system of claim 14, wherein the selected pixel component is a left-hand-most active pixel component.

17. The system of claim 14, wherein the shifted number is one integer greater than the selected number.

18. The system of claim 14, wherein the shifted number is one integer smaller than the selected number.

19. The system of claim 14, wherein the pixel component value comparator is connected to a threshold value register and a pixel value calculator.

20. The system of claim 14, further comprising:

a look-up table containing an expected width E, measured in number of pixel clock pulses, of an expected video image producible by the analog video signal;

a left-hand active pixel status register and a right-hand active pixel status register that respectively determine the horizontal positions of the left-most and right-most pixel components of the active video region;

means for determining an actual width, measured in number of pixel clock pulses, of an actual video image producible by the analog video signal by subtracting the position held in the right-hand status register from the position held in the left-hand status register;

a comparator for comparing the actual width W with the expected width E; and

means for automatically adjusting the clock frequency whenever one of $W > E + 1$ and $W < E$.